

REMARKS/ARGUMENTS

Claims 1-6, 15-26, and 31-38 are currently pending in the present patent application.

In Section 1 of the Final Office Action, the Examiner objects to the drawings for failing to show every feature of the invention specified in the claims. The Examiner states that the limitation of "said floating gate insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions" must be shown or canceled from the claims. The undersigned is puzzled by this objection. Notwithstanding the detailed discussion regarding the terms "lateral," "laterally," "width" direction and direction orthogonal to a plane including the floating gate, source, and drain regions in prior amendments, the Examiner is still apparently not clear on the definition of these terms as used in the present application.

Figures 6-9 of the present application clearly illustrate the limitation recited in the claims and pointed to by the Examiner. As discussed in the prior amendment filed in this application, the term "lateral" or "laterally" corresponds to the sides of the floating gates in a direction extending parallel to the line WL-WL or along a row of memory cells. In other words, the term laterally is in the direction extending parallel to the word lines WL or along rows of memory cells. The claim language pointed to by the Examiner, however, does not merely recite the term "laterally" but more specifically recites the term "insulated laterally." For example, claim 1 recites the "floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer with low dielectric constant value." Thus, the floating gate region is insulated laterally, meaning not that insulation extends along the lateral direction but that the floating gate region is insulated from other floating gate regions adjacent the floating gate region in the lateral direction. At this point in the prosecution this should be manifestly clear to the Examiner. As shown in Figure 9, for example, a first floating gate region FG on the left side of the figure is "insulated laterally" by the low K dielectric layer 9 from a second floating gate region FG shown on the right side of the figure. This first floating gate region FG on the left side of the figure is "insulated laterally" from the second floating gate region FG on the right side of the figure, with the first region being insulated laterally in that the low K dielectric layer 9 is formed between these floating gate regions when progressing from one region to another along the lateral direction.

All elements recited in currently pending claims 1-6, 15-26, and 31-38 are illustrated in the current figures and accordingly no replacement sheets are necessary. If the Examiner is still unclear on this point after considering the above comments, the undersigned requests the Examiner call him to arrange for a telephone interview to discuss this matter and clear up any uncertainty or confusion on the part of the Examiner and thereby further prosecution of the present application.

In Sections 2 and 3 of the Final Office Action, the Examiner rejects claims 1-6, 15-26, and 31-38 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,852,062 to Baker *et al.* ("Baker") in view of U.S. Patent No. 6,800,940 to Catabay *et al.* ("Catabay"). In Section 4 of the Office Action the Examiner provides comments in response to arguments made in the prior amendment. The Examiner correctly indicates that in the prior amendment the "insulators 60 and 64 of [F]igure 11 do not insulate the two floating gates 52 laterally but instead insulate the gates in [a] direction parallel to the plane containing the gate, source and the drain." The Examiner then proceeds to state that this argument is not persuasive because the insulators 60 and 64 "insulate the cells both along the bit line, horizontally and along the word line, as defined in applicants' response." Continuing, the Examiner states that the insulators are shown in a cross-sectional perspective and must extend in three directions. The first of these three directions is termed "laterally" which is said to be "along an axis extending from the source to drain." The second direction is said to be the height of the insulators 60 and 64 and the third direction is said to extend "along the direction of an axis which is orthogonal to a plane containing the gate, source and drain." With regard to this third direction, the Examiner states that "the insulating film composed of the two aforesaid insulators [60 and 64] must has [sic] a width, which is along the axis of the orthogonal."

First, the term laterally as used in the present application is in the direction extending parallel to the word lines WL or along rows of memory cells and NOT "along an axis extending from the source to drain." The Examiner appears to correctly utilize the term "width" as being along the axis of the orthogonal, which corresponds to the direction extending parallel to the word lines WL and thereby in the lateral direction as the term lateral is used in the present application.

Although the insulators 60 and 64 do indeed extend along the lateral direction or width direction and parallel to the word lines WL, this is not the same as the "insulated

laterally" limitation that is expressly recited in pending claim 1. Claim 1 recites the "floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer with low dielectric constant value." Thus, the floating gate region is insulated laterally, meaning not that insulation extends along the lateral direction but that the floating gate region is insulated from other floating gate regions adjacent the floating gate region in the lateral direction by the recited dielectric layer. The insulators 60 and 64 of Baker simply do not insulate laterally the floating gate regions of Baker. The Examiner has pointed to no disclosure in Baker that shows such lateral insulation. In fact, the conventional process utilized in forming floating gates of Baker makes it impossible for the insulators 60 and 64 to insulate laterally the floating gates 52. The undersigned would be more than happy to provide the Examiner with additional details regarding this last point and also to discuss this last point in detail with the Examiner during a telephone interview if the Examiner so desires.

As previously discussed with regard to Catabay, even if low dielectric constant layer 30 is used to replace the layers 60 and 64 these insulators do not insulate laterally the floating gate regions.

Independent claim 15 recites, in part, a memory cell matrix formed on a semiconductor substrate in which adjacent memory cells are coupled to the same word line of the memory cell matrix and are insulated from each other by a dielectric layer with low dielectric constant value. Independent claim 16 recites a memory-cell structure formed on a semiconductor substrate including a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate. Each memory cell in a respective row is coupled to a corresponding word line and each memory cell includes a floating gate region. The memory-cell structure includes an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line.

As discussed above with regard to claim 1, Baker does not disclose such a low dielectric material between adjacent floating gate regions of memory cells coupled to the same word line WL. The layers 60 and 64 are not between the floating gate regions of memory cells coupled to the same word line but instead are between such regions of memory cells coupled to the same bit line (*i.e.*, along the direction BL-BL) and different word lines. As previously mentioned, the conventional process utilized in forming floating

gates 52 of Baker makes it impossible for the insulators 60 and 64 insulate laterally the floating gates 52.

For these reasons, independent claims 15 and 16 are allowable and dependent claims 17-20 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these claims. Independent claims 21, 24, and 31 are allowable for similar reasons to those discussed with regard to claims 1, 15, and 16. All dependent claims not specifically discussed above are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these claims.

New claims 35-38 recite that the low constant dielectric layer completely fills a space between adjacent memory cells coupled to the same word line and each is allowable for the same reasons as the associated independent claim and due to the additional limitations added by each of these dependent claims. The Examiner has once again pointed to no portion of Baker that discloses a low constant dielectric completely filling the space between adjacent memory cells. In fact, the conventional process flow utilized in forming the floating gates 52 of Baker makes it impossible for the low constant dielectric layer to completely fill the space between adjacent memory cells that are coupled to the same word line. Such conventional process flows as in Baker simply would not allow the same dielectric of the insulators 60, 64 to be present between adjacent floating gate regions in the lateral direction along the word lines (*i.e.*, to insulate laterally the floating gate regions). Once again, the undersigned would be more than happy to provide the Examiner with additional details regarding this last point and also to discuss this last point in detail with the Examiner during a telephone interview if the Examiner so desires.

Please note that minor amendments to specification were made to change terms used in these paragraphs to be consistent with terminology used in the remainder of the application. None of these amendments introduces new matter into the application.

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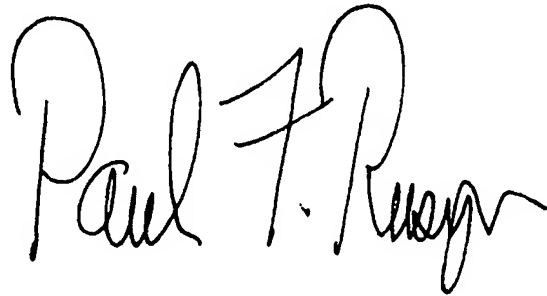
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The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.** If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

A handwritten signature in black ink, reading "Paul F. Rusyn". The signature is fluid and cursive, with the first name "Paul" being the most prominent.

Paul F. Rusyn
Registration No. 42,118
155 – 108th Avenue NE, Suite 350
Bellevue, WA 98004-5973
(425) 455-5575 Phone
(425) 455-5575 Fax